Z transform elements – Part 2:

About the writer: Harvey Morehouse is a contractor/consultant with many years of experience using circuit analysis programs. His primary activities are in Reliability, Safety, Testability and Circuit Analysis. He may be reached at harvey.annie@verizon.net. Simple questions regarding my articles for which I know the answer are free. Complex questions, especially where I am ignorant of the answers, are costly!!!

Summary:

This document will be in several parts, where this is part 2. Difference equations involve expressions that have meaning at discrete time intervals – sampled data systems. Generally this involves the use of A/D converters, digital processing functions, and D/A converters. They are also useful in describing switched capacitor systems.

To develop models that enable one to analyze such systems in a (SPICE) continuous time domain (transient analysis) and also in the frequency domain (AC analysis) with one set of models is the goal. Here we develop models for a Sample and Hold function.

Sampled Data Systems:

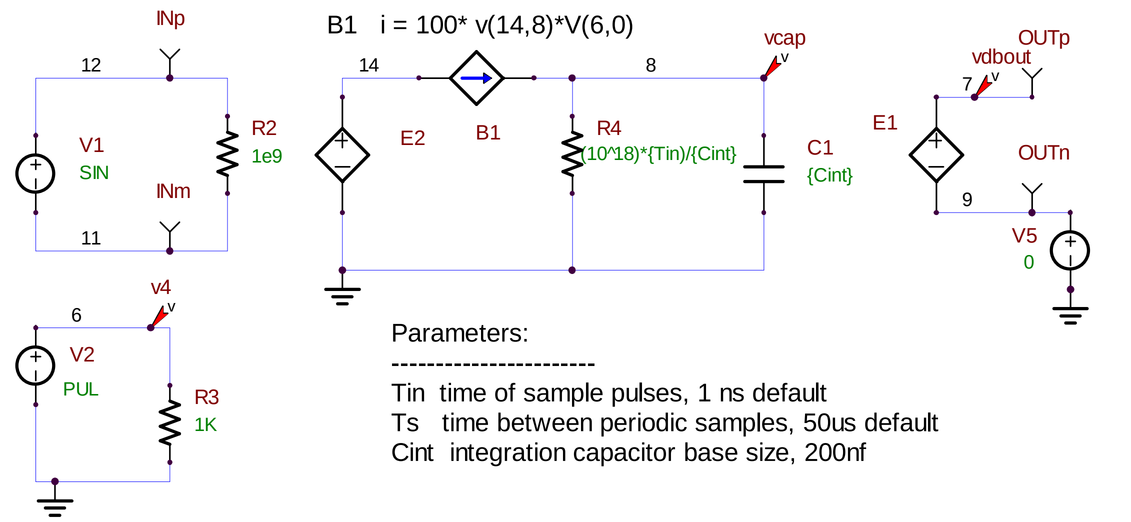
There are several different ways to solve difference (not differential) equations. These implementations often are combined in a system with analog circuitry. It would be useful to be able to able to accommodate both sampled data and continuous time circuitry analysis within one solution environment such as SPICE. And with the proper Z transform elements this is possible and feasible. Like the familiar Laplace 's' transform, the Z transform element can also be used within SPICE.

Sample and Hold device modeling 1

A Sample and Hold (SOH) device is useful in providing an essentially static output from a sampled input. This allows time (and also Z) domain simulation to occur during the intervals between sampling events. (It is hoped that such a device model will operate correctly, or nearly so during an AC and DC simulation also.)

What this device does is to create a static output from a sampled input that remains essentially constant until the next sample period. This would allow digital logic (if any) to be use to operate on the signal, the analog value to be processed by an A/D converter, or other operations to occur. Alternately, were Z domain operations to occur with a signal, this would extract the correct value of the output(s) at the sample time.

The operation can best be seen with a model, as shown in Figure 1.

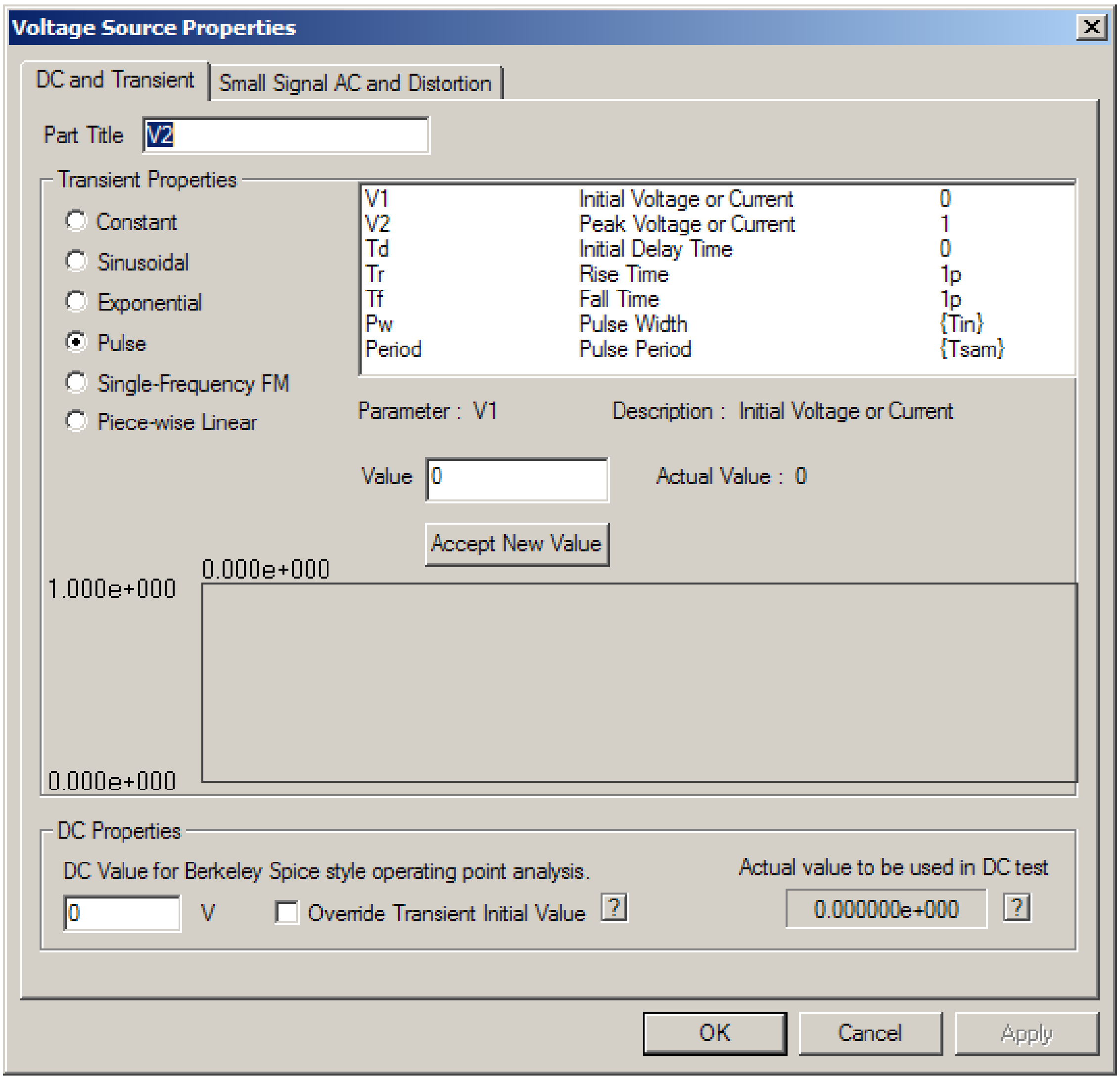


SnH1 device circuit1
Figure 1

The circuit in Figure 1 takes the value of the input voltage V1 and buffers it with device E2, a voltage to voltage converter, providing the sampled voltage to which capacitor is desired to charge to at the sampling instant. Current source B1 measures the difference between the sampled voltage and the output voltage, and provides a current to C1 to charge (or discharge) it to the correct voltage at the sampling instant..

B1 current is scaled up by a factor of 100 to charge capacitor C1 rapidly, with C1 being nominally small for the same reason. The resistance of R4 is scaled by the inherent equation to eliminate the need for super large resistors, but provide a real, but large value resistance to make the discharge time constant of C1 negligible in most instances.

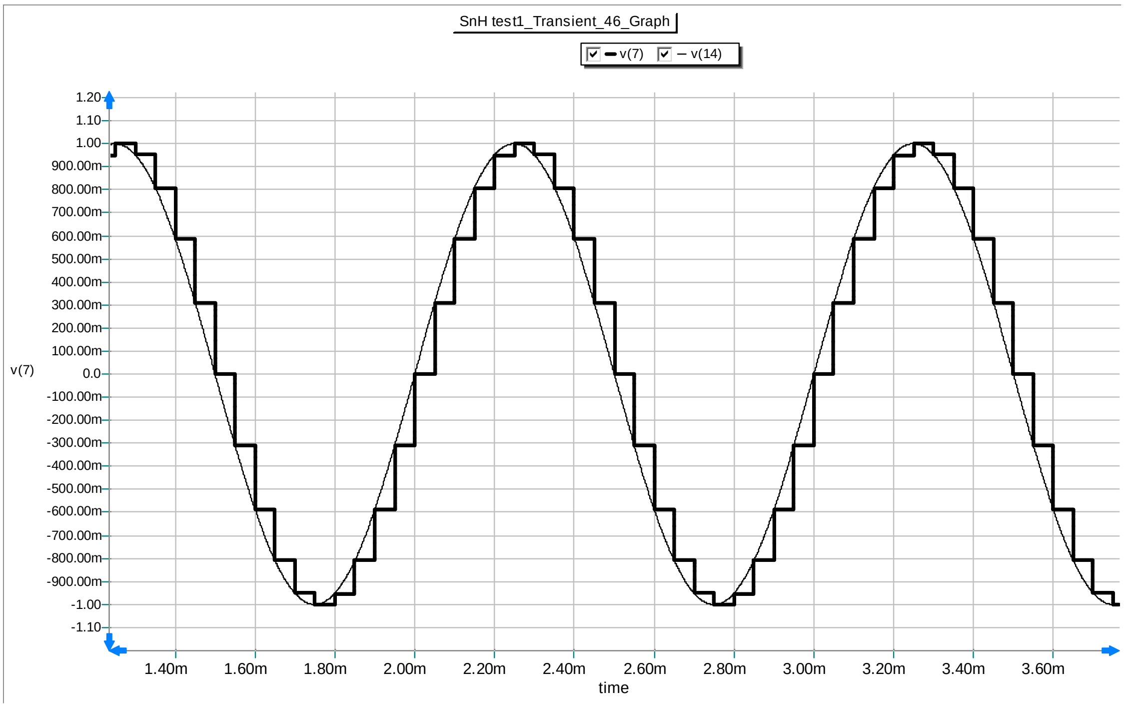
The settings for the V2 pulse generator are interesting. This is shown in Figure 2 following.



SnH1 device circuit1pulse settings
Figure 2

The settings for source V2 pulse rise and fall times are small, but they could actually be zero valued, clearly an impossibility. **What will happen is that SPICE will use the smallest value it can for these parameters. When this window is closed, SPICE will protest that the value of pulse width cannot be zero, but this may be ignored.**

Performing a transient simulation of this circuit with an AC input of 1kc, 1v provided by V1, the resultant output is shown in Figure 3.



SnH1 device circuit1transient output
Figure 3

In Figure 3 the input signal and the sampled output are shown. It should be apparent that there is a time delay between the ‘average’ sampled output and the input. This delay, a phase shift, could be meaningful in a feedback circuit.

The next test is to perform an AC small signal frequency sweep of the circuit. This is not shown, but the result is a 0 db gain (or loss) over frequency. Why does this not show aliasing effects when the input signal frequency approaches and exceeds the Nyquist frequency? Think about this a bit.

The reason is that an AC analysis is a linearized analysis of the circuit about a small signal operating point. This analysis is performing a linear analysis where no new frequencies are generated. Looking at it another way, no sampling can occur as the pulse generator is disabled in an AC analysis. The current generator B1 is always disabled.

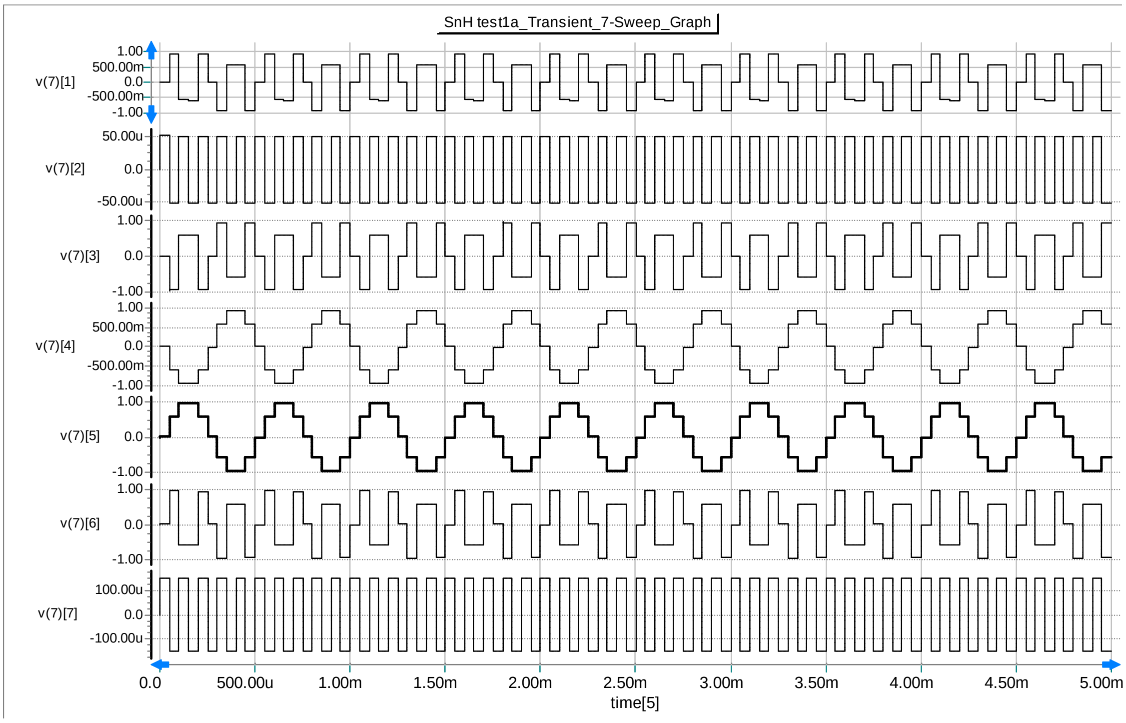
Now the voltage of E1 (AC) MUST be dropped across the B1 current source and the parallel combination of R4 and C1 WITH no current flowing. This can only occur if the voltage across B1 is zero and E1 volts are present across R4 and C1. Thus the output voltage must equal the input voltage. But what about the current through R4?

Well, let us see what SPICE says about the currents. This can be done by plotting the currents on the sweep waveform. Placing an ammeter in series with R2, and performing another sweep with these changes produces the result (not shown) that R2 passes no current, and E2 produces effectively no current as well.

The answer is that SPICE produces a solution at EACH frequency point, and not in between. ***The DC operating point is zero***. ***About*** that operating point, the small signal gain is unity, as the output is constrained to be equal to the E1 voltage. It is strange, but that is what happens.

Now the question arises, does the circuit really work if the Nyquist sampling effects are not seen?

First, remember that sampling is a nonlinear process. New frequencies are created. That being so, a transient solution should show these effects. A transient sweep will be performed, with a stepped frequency input. This output is shown in Figure 4.



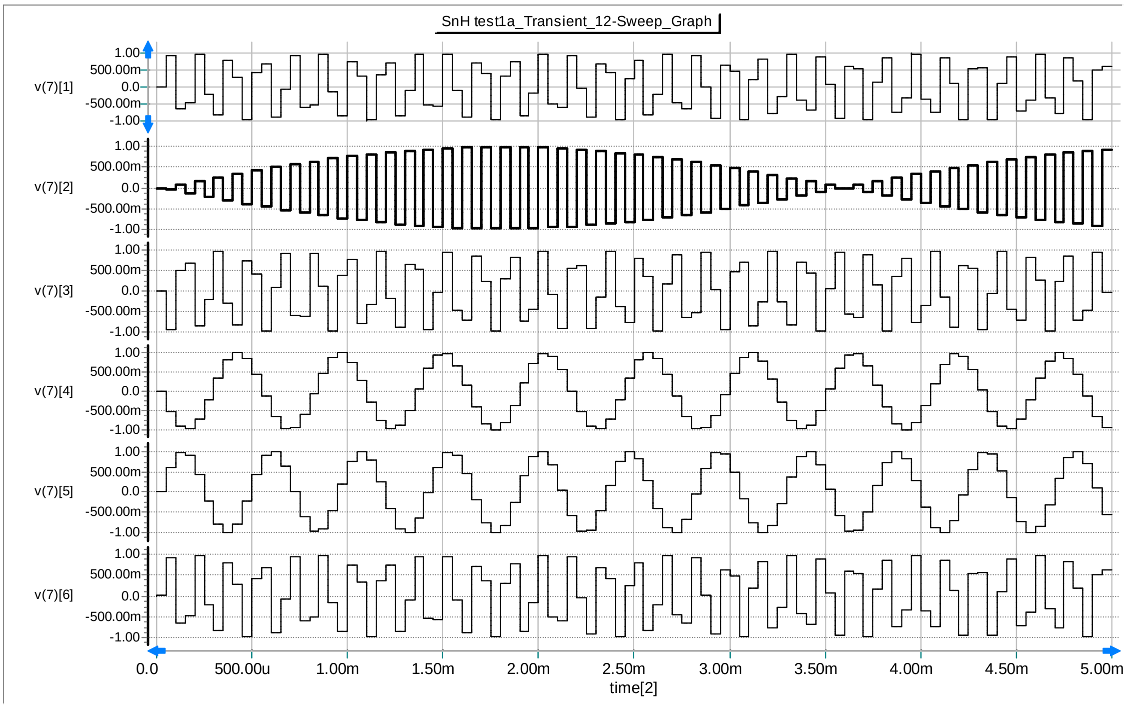
SnH1 device circuit1transient sweep output

Figure 4

In Figure 4 the sweep outputs are with inputs of 6, 10, 14, 18, 22, 26 and 30Kc, from top to bottom. With a sampling period of 50 us, the sampling frequency is 10 kc. The Nyquist sampling frequency where folding starts is at 5 kc, where there are two samples per input period. This is seen in the first curve v(7)(1) where there are less than two samples per input period, and the waveform is 'distorted', and lowered in frequency.

The second curve, V(2)(2), it should be noted, has an amplitude of about 50 uv, and is at the sampling frequency. This 'mirroring' is shown by the curve V(7)(7), both being symmetrical in difference about the 10 kc sampling rate. Similar 'mirroring' is seen in V(7)(4) and V(7)(5) and also by V(7)(3) and V(7)(6).

Now of course the signals and sample period frequencies are related by integers. It is instructive to change the sweep starting frequency such that no even multiples occur. The starting sweep input frequency was thus changed in frequency to 2.137l Hz (arbitrarily). The result is shown in Figure 5.



SnH1 device circuit1transient sweep output2
Figure 5

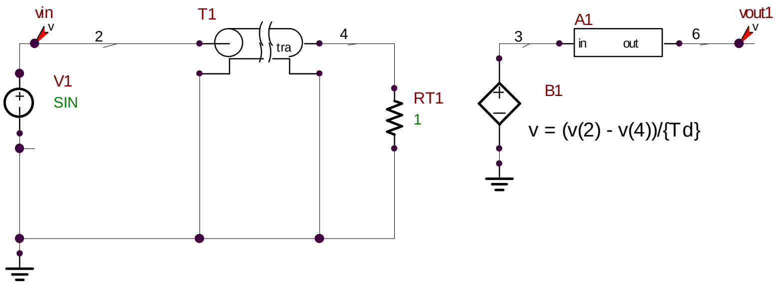
In Figure 5 the effect of non-synchronous input signals are seen in the results. Depending on the frequency offsets, a variety of results may be seen. This illustrates the nonlinearity of the realization.

The device model is useful for signals below the Nyquist criterion however, but it does not work quite as we might like, or think we would like, in an AC simulation.

Sample and Hold device modeling 2

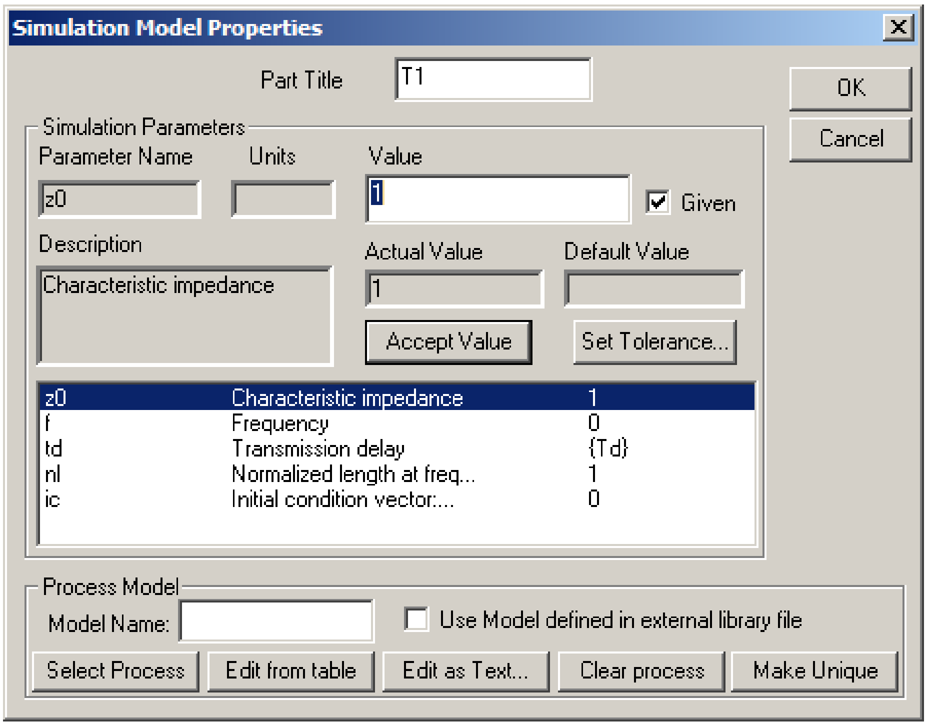
Another way to model a SnH device is using Z transforms and with Laplace operators.

It can be shown that the SnH transfer function is equal to $(1 - z^{-1})/(Td*s)$. Now as z^{-1} is a linear function, we should be able to model a sample and hold circuit that works for AC (hopefully). With an integrator and the equivalent of the z^{-1} element (zn1) as previously created in part 1this should be possible.



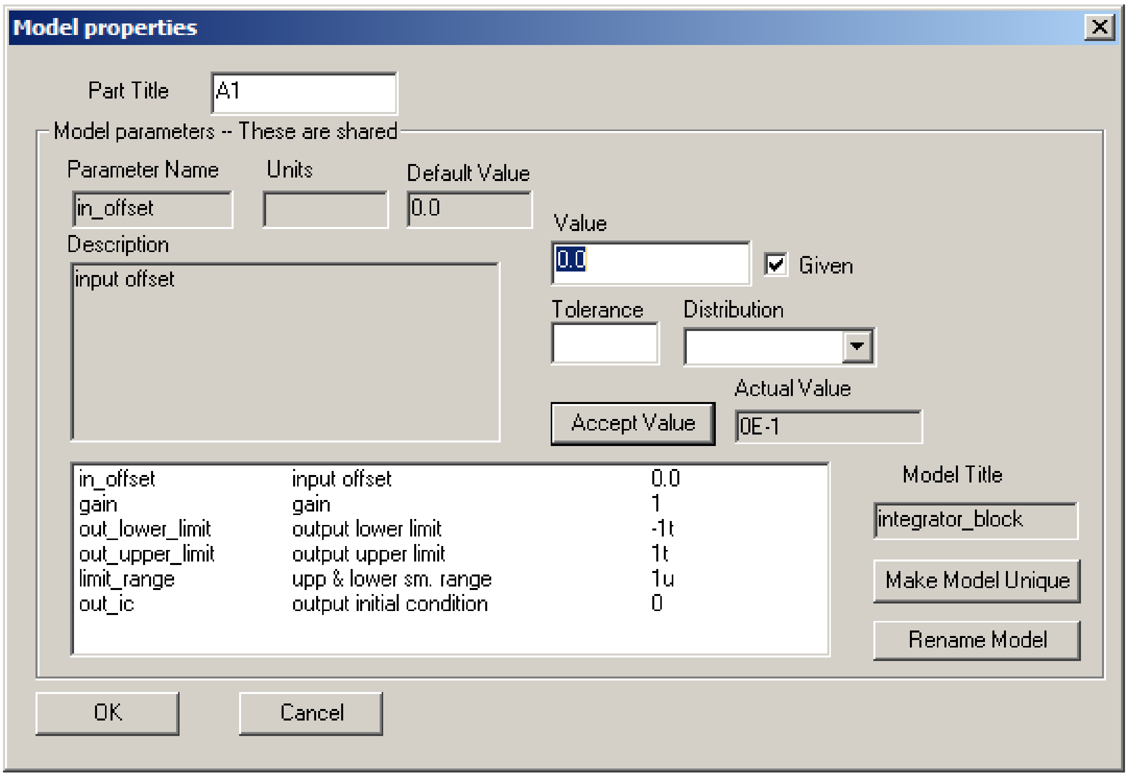
SnH2 device circuit1
Figure 6

V1 provides a 1k, 1v sine wave input. The settings for the transmission line are shown in Figure 7 following:



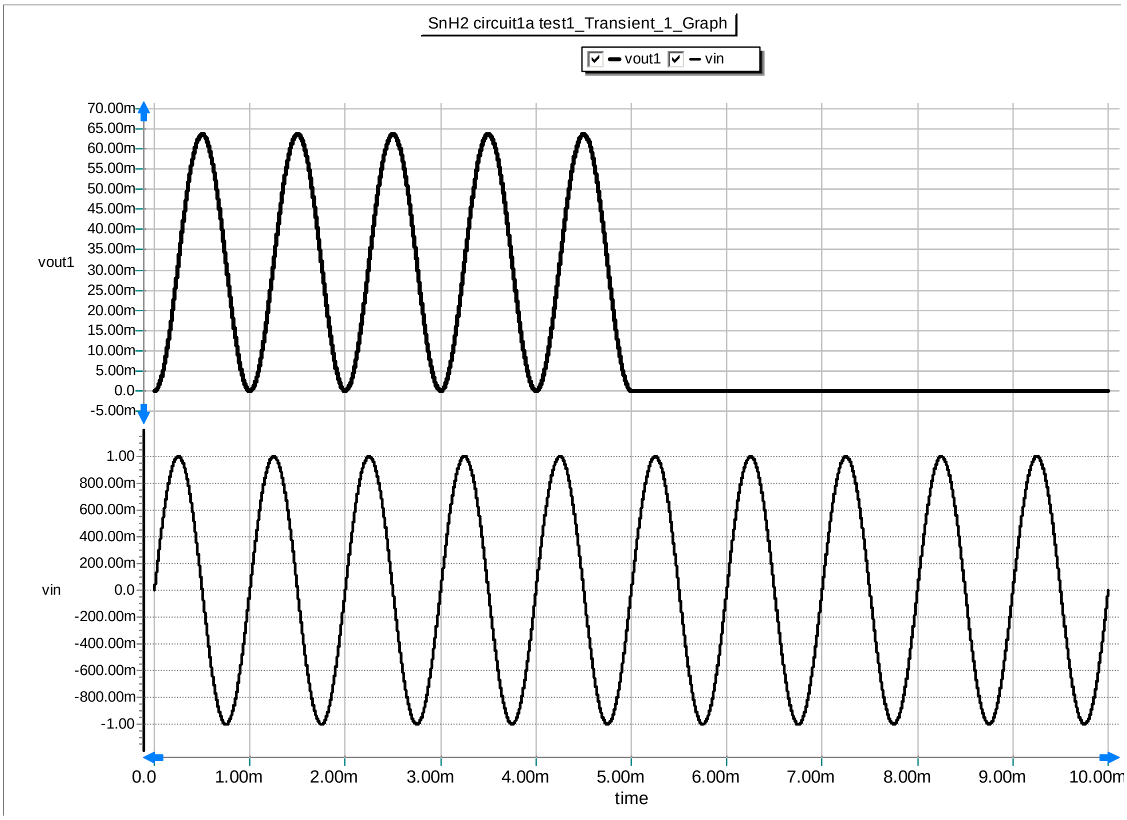
SnH2 circuit1 transmission line settings
Figure 7

Device A1in Figure 6 is an integrator device. Its settings are shown in Figure 8.



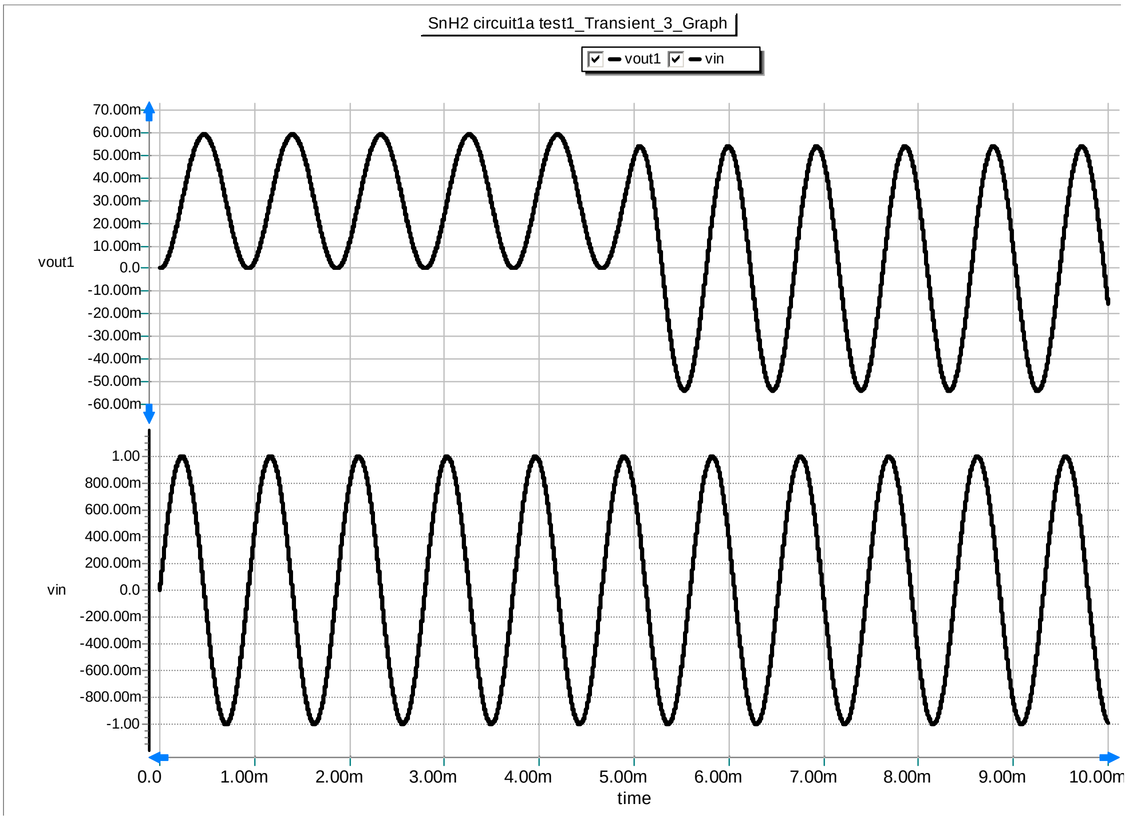
SnH2 circuit1 integrator device settings
Figure 8

Performing a transient analysis of the circuit the curve of Figure 9 results.



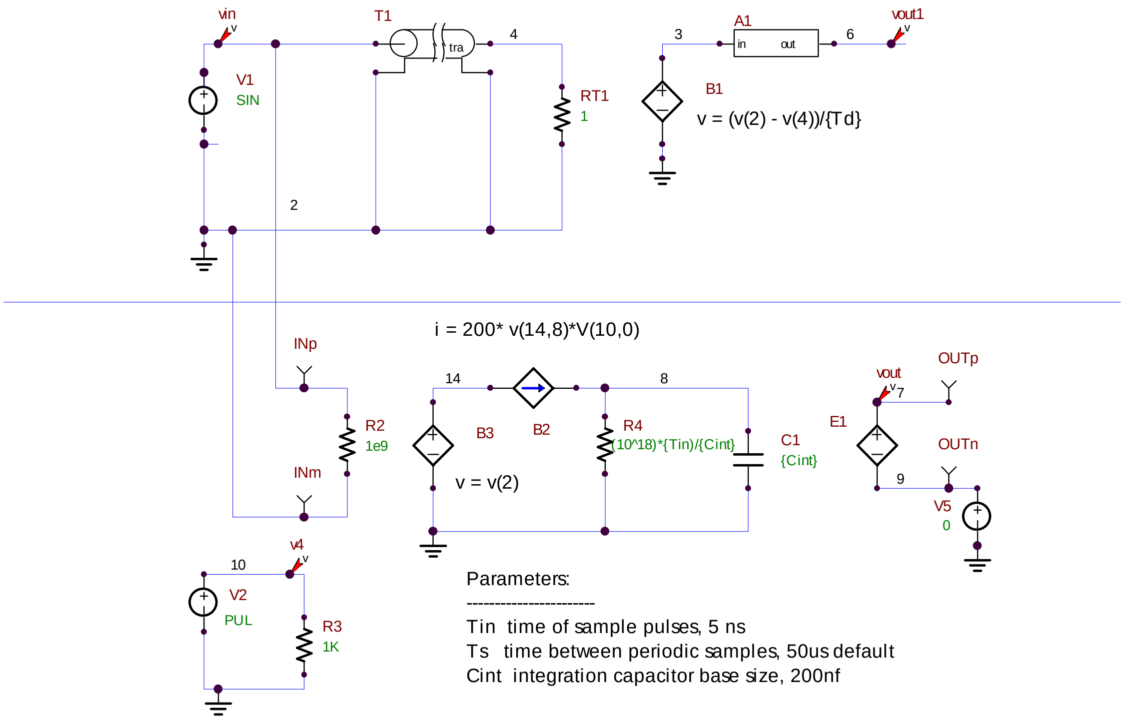
SnH2 circuit1 transient test1
Figure 9

In Figure 9 it can be seen that the output is ‘blanked’ after the delay time. ***<u>Or is it</u>***? As the delay is exactly 5 cycles of the input, the sum of vin and the delayed vin is indeed zero after the delay time has elapsed, however if the delay is not an integer multiple of the input signal period this will not be so. Changing the input frequency to 1.073 kc, the curve in Figure 10 is produced.



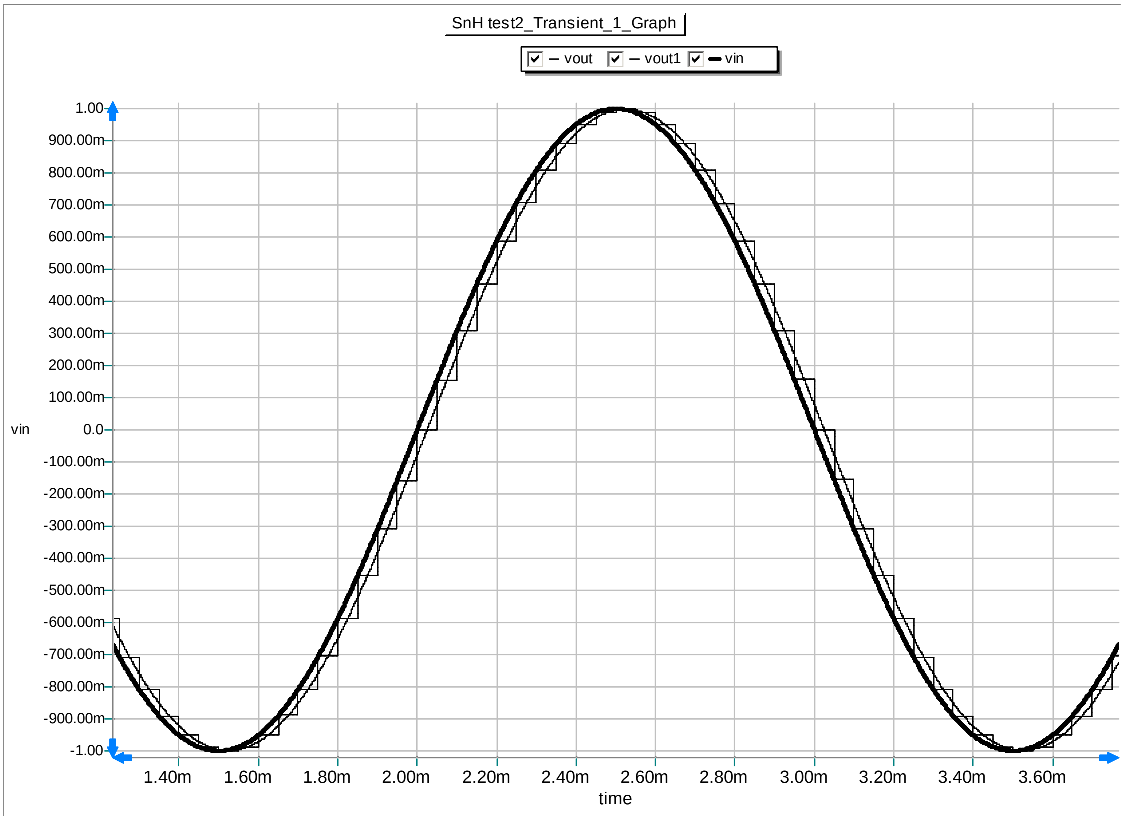
SnH2 circuit1 transient test1a
Figure 10

The question now arises why the performance of the SnH2 circuit is so different than that of the SnH1 circuit in a transient analysis? The answer is that it is not. The difference is in the choices of values of some of the parameters. This will be seen shortly. Refer to the circuit of Figure 11 following.



SnH2 circuit2
Figure 11

In Figure 11 are shown the SnH2 circuit (above the dividing line) and the SnH1 circuit below. The outputs transient performance with a 500 cps sine wave input is shown in the graph of Figure 12.



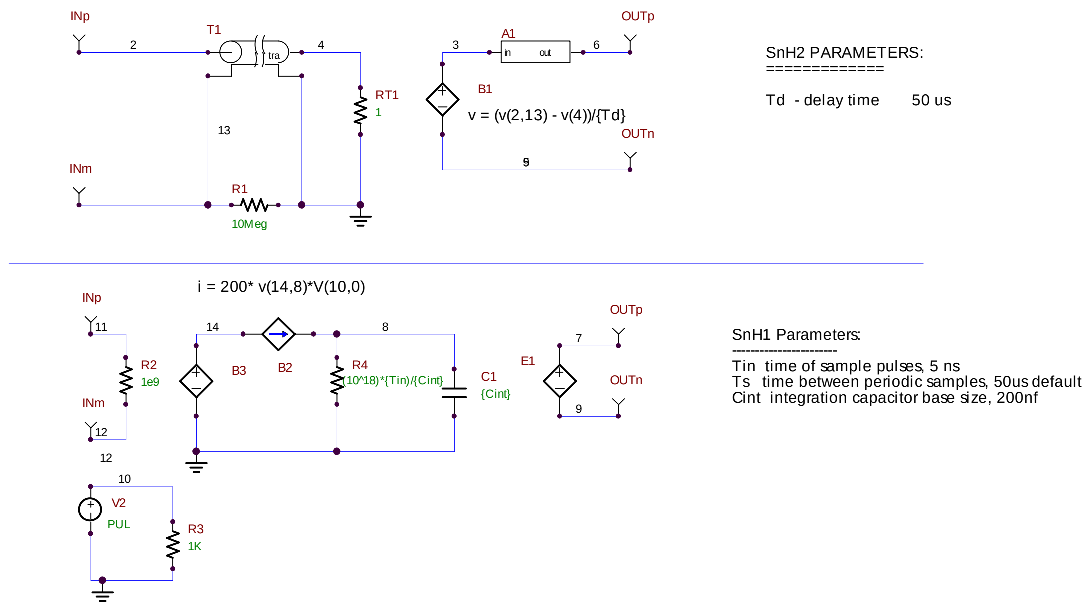
SnH2 circuit2 transient graph
Figure 12

In Figure 12 the bold curve is the input waveform. The stepped waveform is the SnH1 circuit output, while the lagging sinusoidal waveform is the SnH2 output. Note that the SnH2 output is an 'average' of the SnH1waveform. The delay can be seen to be equal to Td*fs*360 degrees, in this case it is (50^-6)*500*360, or 9.0 degrees, but of course the phase shift varies with the input signal frequency.

But the SnH2 circuit is not a sample and hold, you say!! Well it is, however the hold time is essentially zero, or as near to zero as the SPICE circuit engine numerical solution will achieve. To use this circuit in a sample and hold manner, after the signals are processed with various 'z' and time dependent circuits, it may need to be processed to restore the final sampled signal output to one whose value is f(Td).

Now note that the output loading is unchanging. Suppose that the input voltage and the output loading both vary with time. This is the case with a switched capacitor voltage supply and with a switched capacitor circuit in general. This is a more complex situation, and the switched capacitor voltage inverter circuit will be covered in another part.

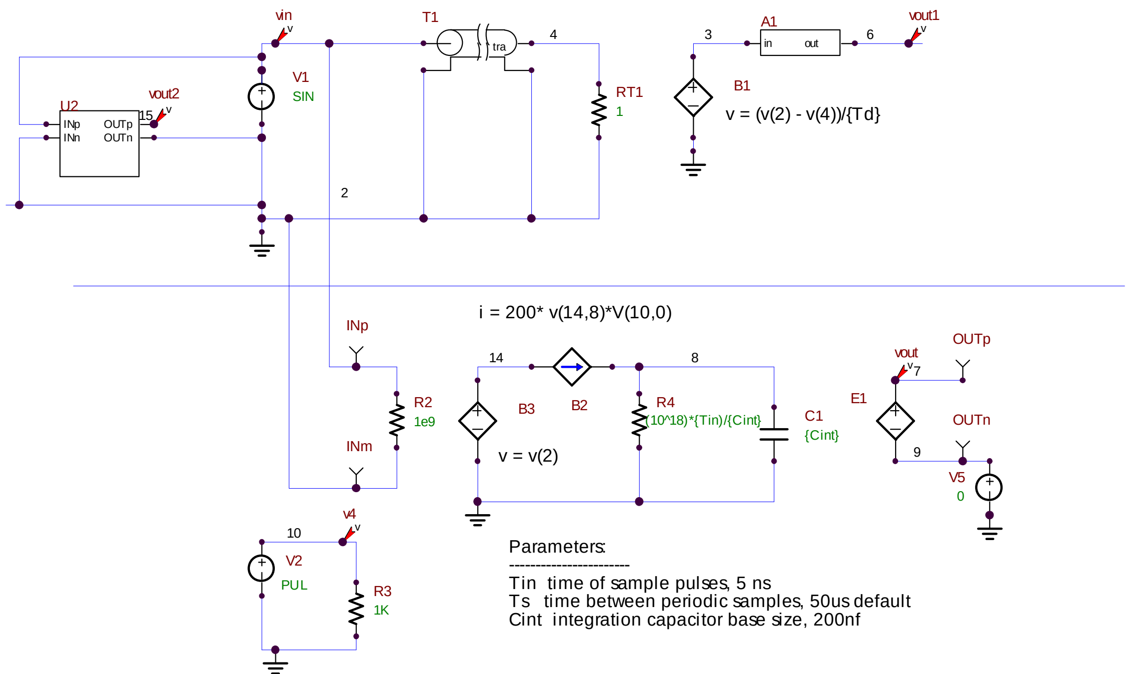
For now, we need to create circuits for the SnH1 and SnH2 models. These device models are shown in Figure 13.



SnH models
Figure 13

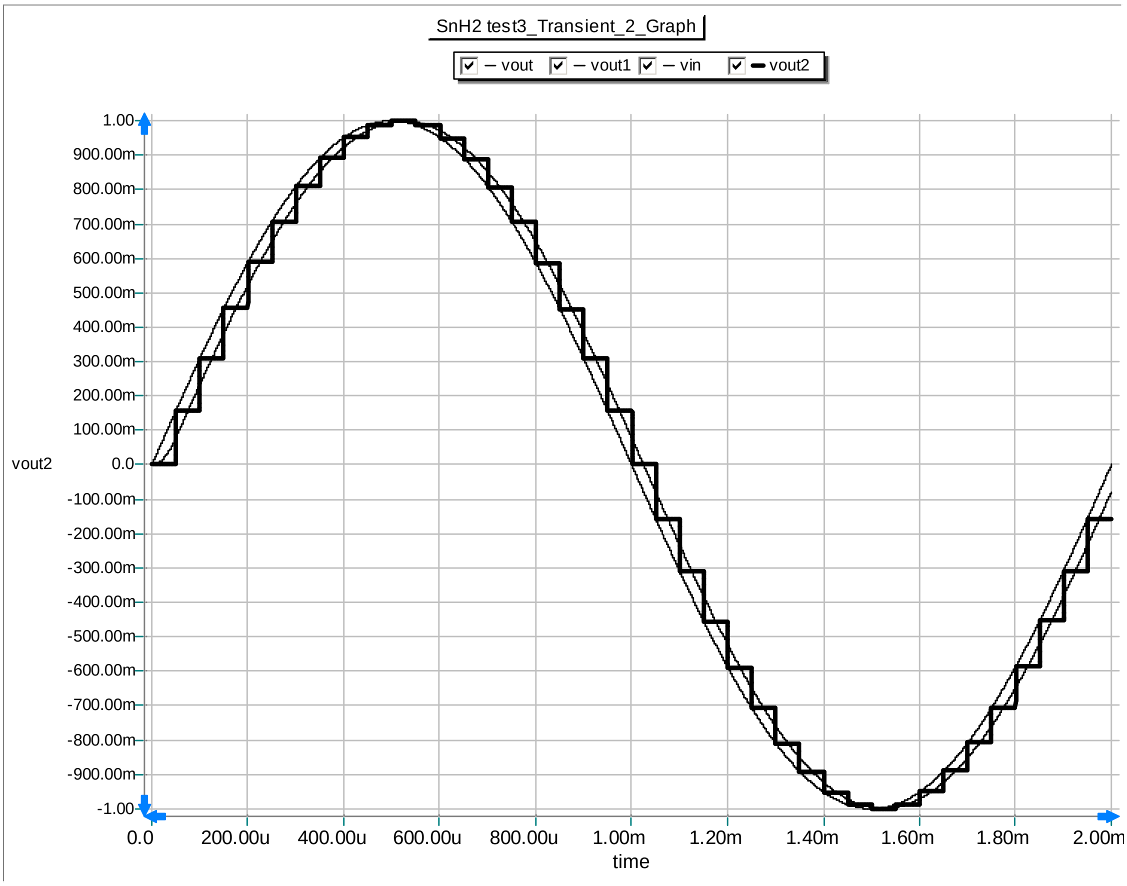
The two models created are isolated versions. The input and outputs can be isolated.

The device model for the SnH1 device in a test circuit with the primitive device models is shown in Figure 14.



SnH1 model test 3
Figure 14

Device U2 is a SnH1 device. A transient analysis of the circuit if Figure 14 is shown in Figure 15.

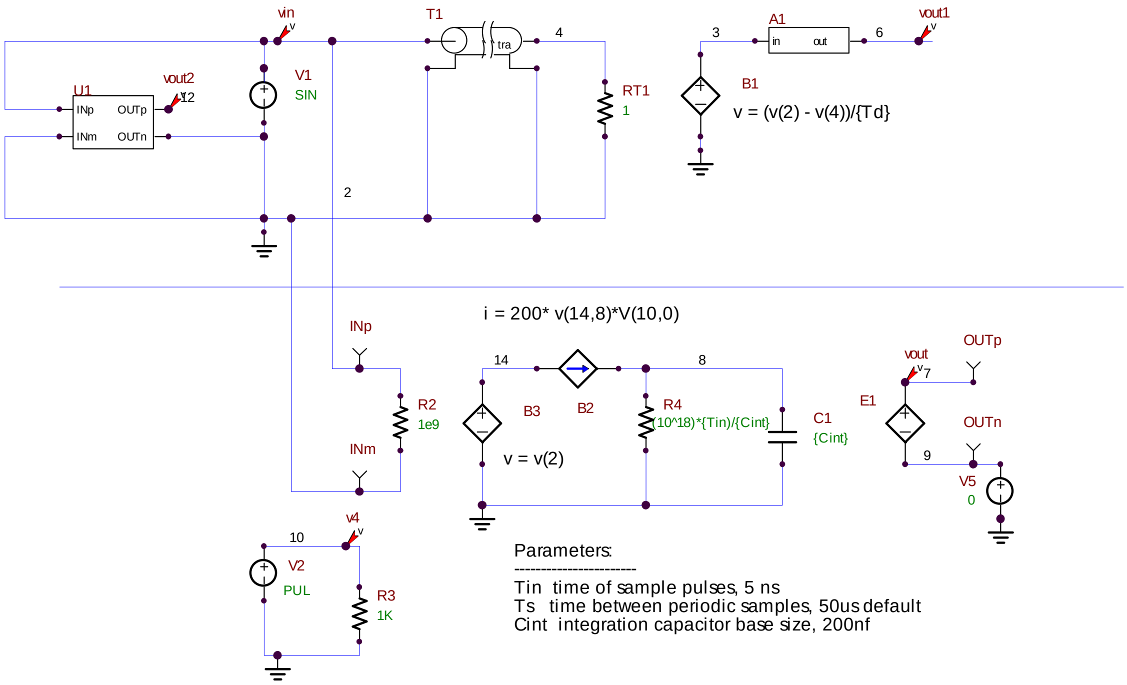


SnH1 model transient test 3

Figure 15

In Figure 14 there are two identical stair-step curves shown that are identical, which are the vout and the vout2 curves of the SnH1 type circuits. The leading sinusoidal type waveform is the input voltage.

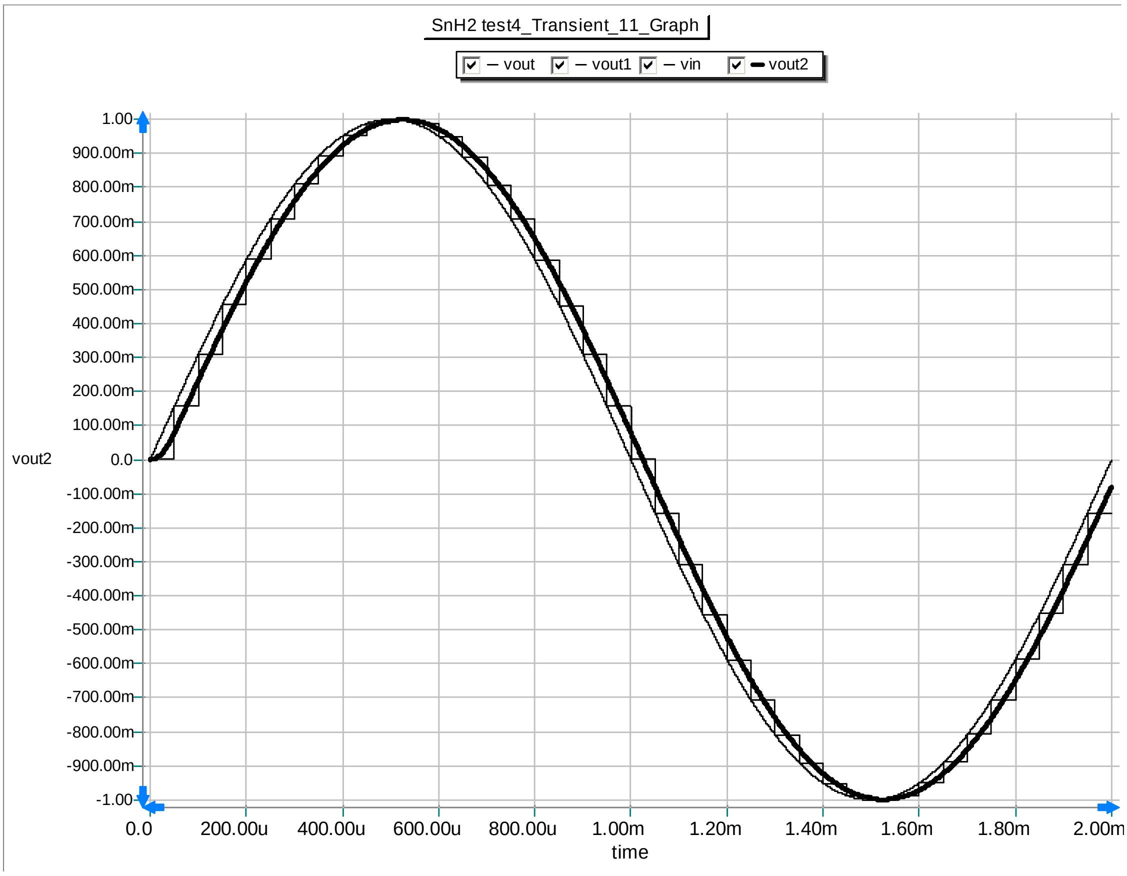
The test circuit for the SnH2 device is shown in Figure 16 following.



SnH2 model test 4

Figure 16

The transient test results for the circuit of Figure 16 is shown in Figure 17.



SnH2 model transient test 4
Figure 17

In Figure 17 the bold curve is that of the vout1 and vout2 SnH2 device curves, which agree.

Having arrived at two device models, the questions arise as to which should be used and when?

Certainly if a DC or AC analysis is to be performed, the SnH2 device provides more accurate results, at least for signals below the Nyquist sampling frequency value. Yet the actual circuit might contain a sampling scheme that is comparable to charging and discharging a capacitor, and real time circuitry might be sensitive to the nonlinearities and new frequencies presented by this operation.

The SnH1 device allows one to edit and change the initial value of the integration capacitor voltage (by editing the model), and this could be useful in some instances. Enough perhaps to justify even adding this value as a user defined parameter.

Moreover, the SnH1 switch time and capacitor value may need to be altered to enable proper results to occur with a given application.

There are many interesting and useful areas that could be covered. Namely pre-distortion of the sampled signal to minimize the effects of the sampled data waveform apparent phase shift by the sampling process.

Interesting topics include pre-filtering of the waveform to be sampled if there are signal components near and past the Nyquist frequency, which could be indistinguishable at the output from the results of lower frequency inputs.

Basically there are three ways to analyze a circuit, the time and frequency domain being most familiar. The Z domain could be useful as a third method in certain cases.

Conclusions:

Two different SnH realizations have been created, that may be used in the analysis of sampled data, difference equation circuits. The SnH2 realization will work in AC, DC and transient simulations.